CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1 (currently amended). A circuit for driving a link being programmable by an energy pulse, the circuit generating an output signal with a boosted signal level compared with a logic level of an input signal, the circuit comprising:

an input stage having a first input terminal pair for receiving a first input signal with a logic level, and a second input terminal pair for receiving a second input signal with a logic level, said input stage having a first switch pair with control inputs forming said first input terminal pair, said input stage having a second switch pair connected to said first switch pair for forming a logic combination of the first and second input signals, said second switch pair having control inputs forming said second input terminal pair; ~~and~~

an output stage connected to said input stage and having a terminal for feeding in a blowing voltage, a first supply voltage terminal, and an output terminal coupled to the link

and the output signal with the boosted signal level is ~~can be~~ tapped at said output terminal; and

a switch having a control input and a controlled path with a first terminal connected to said terminal for feeding in the blowing voltage and a second terminal connected to the link, said control input of said switch connected to said output terminal of said output stage and, depending on the first and second input signals, said switch through-connects said first terminal of said controlled path, connected to said terminal for feeding in the blowing voltage, to said second terminal of said controlled path connected to the link.

2 (canceled).

3 (original). The circuit according to claim 1, wherein said first switch pair has two input transistors including a first input transistor driven by the first input signal and a second input transistor driven by an inverted first input signal.

4 (original). The circuit according to claim 3, wherein said output stage includes two cross-coupled transistors coupled to said input transistors.

5 (original). The circuit according to claim 4, wherein said output stage further includes two further transistors having control inputs connected to said first supply voltage terminal, said two further transistors coupling said cross-coupled transistors to said input transistors.

6 (original). The circuit according to claim 3, wherein said second switch pair includes two further input transistors including a third input transistor driven by the second input signal and a fourth input transistor driven by an inverted second input signal.

7 (original). The circuit according to claim 6, wherein said first and fourth input transistors are connected up in parallel with one another, and said second and third input transistors are connected in series with one another and said first, second, third and fourth transistors form an AND combination.

8 (original). The circuit according to claim 6,

wherein said third and fourth transistors have control inputs; and

further comprising a shift register generating the second input signal and the inverted second input signal and connected to said control inputs of said third and fourth input transistors for transmitting the second input signal and the inverted second input signal.

9 (original). The circuit according to claim 3,

wherein said first and second transistors have control inputs; and

further comprising a volatile memory cell providing the first input signal and the inverted first input signal and connected to said control inputs of said first and second input transistors for transmitting the first input signal and the inverted first input signal.

10 (original). The circuit according to claim 1, wherein the circuit configuration is constructed using CMOS circuit technology.